REMARKS/ARGUMENTS

Claims 1-20, 27, and 31-46 are pending in the application. Claims 1, 16, 38, and 46 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 3 of the office action, the Examiner rejected claims 1-11, 16-20, 38, 44, and 46 under 35 U.S.C. 102(b) as being anticipated by Shou. In paragraph 6, the Examiner rejected claims 12-15, 27, and 31-32 under 35 U.S.C. 103(a) as being unpatentable over Shou in view of Black. In paragraph 7, the Examiner rejected claims 33-37, 39-43, and 45 under 103(a) as being unpatentable over Shou in view of Zhou. For the following reasons, the Applicant submits that all of the pending claims are allowable over the cited references.

Claims 1 and 16

Claim 1 is directed to a digital filter comprising at least two multiple stage shift registers, a plurality of multipliers; a tap weight shifter, and an adder. The plurality of multipliers correspond in number to the total number of stages in the at least two multiple stage shift registers, where each multiplier receives as a first input an output from a stage of the at least two multiple stage shift registers. The tap weight shifter is coupled to a tap weight source to receive tap weights, where the tap weight shifter is coupled to provide a second input to each multiplier. The tap weight shifter is capable of shifting tap weights, and each multiplier produces an output corresponding to a product of the first and second inputs. The adder sums the multiplier outputs to provide a sum output. Two or more sum outputs are generated by the adder between consecutive shiftings of new data into the at least two multiple stage shift registers. No new data is shifted into any of the at least two multiple stage shift registers between generation of a first of the two or more sum outputs by the adder and a last of the two or more sum outputs by the adder. The Applicant submits that Shou does not teach or even suggest such a combination of features.

The Applicant submits that the Examiner mischaracterized the teachings of Shou in rejecting claim 1. In particular, on page 2, the Examiner stated that Shou teaches, in Fig. 1, "M (M>2) N (N>2) stages shift-register," citing element **3** and column 8, lines 62-64. The Applicant assumes that the Examiner believes that element **3** in Shou's Fig. 1 is an example of the "at least two multiple stage shift registers" of claim 1. However, Shou's element **3** in Fig. 1 is not "at least two multiple stage shift registers"; element **3** is a single multi-stage shift register in which each stage stores a single M-bit digital data value. Column 8, lines 62-64, explicitly states that "reference numeral **3** denotes an N-stage shift register for storing M-bit digital data from A/D converter **2** in each stage at every sampling timing." (emphasis added) Thus, the Examiner mischaracterized the teachings of Shou in suggesting that Shou teaches more than one shift register.

Furthermore, on page 3, the Examiner stated that Shou teaches, in Fig. 2, "more than one sums generated by adder 7_i to 7_M in one cycle of spread code (in chip rate)." The Applicant assumes that the Examiner believes that elements 7_1-7_M in Fig. 2 constitute an example of the adder of claim 1. According to claim 1, "two or more sum outputs are generated by the adder between consecutive shiftings of new data into the at least two multiple stage shift registers." Here, too, the Applicant submits that the Examiner mischaracterized the teachings in Shou. Significantly, elements 7_1-7_M are not a single adder that generates M outputs; they are M adders, each of which generates a single output. For example, column 9, lines 52-53, refers to "adders 7_1 to 7_M.," and column 9, line 60, refers to "Each adder 7_j." (emphasis added) Moreover, each adder 7_i generates only a single output between consecutive shiftings of new data into shift register **3**. Thus, the Examiner mischaracterized the teachings in Shou in

suggesting that Shou teaches that "two or more sum outputs are generated by the adder between consecutive shiftings of new data into the at least two multiple stage shift registers."

None of the other cited references of record teach these features of claim 1 that are missing from Shou.

For all these reasons, the Applicant submits that claims 1 and 16 are allowable over the cited references. For similar reasons, the Applicant submits that claim 16 is allowable over the cited references. Since claims 2-15, 17-20, 27, and 31-32 depend variously from claims 1 and 16, it is further submitted that those claims are also allowable over the cited references.

Claim 33

According to the method of claim 33, (a) digital data is shifted into first and second multiple stage shift registers, (b) an output from each stage of the first and second multiple stage shift registers is multiplied by an associated, respective tap weight to produce a plurality of products; (c) the plurality of products are combined to form a sum, (d) the tap weights are circularly shifted, and (e) steps (b) and (c) are repeated at least once before step (a) is repeated.

In rejecting claim 33, on page 4, the Examiner suggested the same mischaracterization that Shou teaches more than one multi-stage shift register. See previous discussion of claims 1 and 16.

Furthermore, the Examiner stated on page 5 that, in Shou: "The multiplying with proper Spread Code, summing, and providing the proper Spread Code for multiplying in the single spread code cycle are repeated before the next input clocking into the shift register 3, then start filtering the next input in the next clk." Significantly, however, the Examiner provides no citation to any specific teaching in Shou in support of this statement. In fact, Shou provides no such teaching. Here, too, the Applicant submits that the Examiner mischaracterized the teachings of Shou.

None of the other cited references of record teach these features of claim 33 that are missing from Shou.

For all these reasons, the Applicant submits that claim 33 is allowable over the cited references. Since claim 34 depends from claim 33, it is further submitted that claim 34 is also allowable over the cited references.

Claim 35

According to the method of claim 35, (a) data is shifted into N multiple stage shift registers, each of the N multiple stage shift registers having at least L stages, N and L being integers, N being at least 2, (b) an output from each of the at least L stages of the N multiple stage shift registers is multiplied by a corresponding tap weight to produce a plurality of products, (c) the plurality of products are combined to form a sum, (d) the tap weights are circularly shifted, (e) steps b, c, and d are repeated N-2 times before step a is repeated, and (f) steps b and c are repeated again before step a is repeated.

For at least some of the same reasons that claim 33 is allowable over the cited references, the Applicant submits that claim 33 is allowable over the cited references. Since claims 36-37 depends from claim 35, it is further submitted that those claims are also allowable over the cited references.

Claims 38 and 46

According to claims 38 and 46, the digital filter has $N>1$ multiple-stage shift registers, a tap changer, a plurality of multiplying elements, and an adder, where the adder is adapted to generate two or more sums for each set of data stored in the shift registers. For at least some of the same reasons provided earlier, the Applicant submits that claims 38 and 46 are allowable over the cited references. Since claims 39-45 depend variously from claim 38, it is further submitted that those claims are also allowable over the cited references.

Claim 44

According to claim 44, the N multiple-stage shift registers do not all have the same number of stages. For example, in the embodiment shown in Fig. 4 of the present application, shift registers $\mathbf{464}_1$ and $\mathbf{464}_2$ each have L+2 stages, while shift registers $\mathbf{464}_3$ and $\mathbf{464}_4$ each have only L+1 stages. Thus, in this particular example of claim 44, the $N=4$ multiple-stage shift registers do not all have the same number of stages.

In rejecting claim 44, the Examiner stated that Shou teaches "the M multiple-stage shift registers having MxN stages which is not a fix number, the number of M is by design choice (column 9 lines 12-16). Hence the M multiple-stage shift registers do not have the same number of stages." The Applicant submits that the Applicant has again mischaracterized the teachings in Shou. The Examiner has also confused the concept of the number of shift registers with the concept of the number of stages in each shift register.

In Shou, N is the number of stages in shift register **3**, while M is the number of bits per digital datum in each stage of shift register **3**. The Applicant assumes that the Examiner believes that Shou teaches M shift registers, each with N stages. Assuming for the sake of argument that the Examiner's belief is correct (which the Applicant denies), in order for Shou to teach an example of claim 44, Shou would have to teach that one or more of the M shift registers had a number of stages other than N. Clearly, however, Shou provides no such teaching.

Column 9, lines 12-16, of Shou teaches that different embodiments can have different numbers of bits (M) per stage. That is not the same thing as teaching that a single embodiment can have different numbers of bits per stage. In fact, Shou's invention would not even work if the number of bits per stage were to vary over the shift register.

Thus, the Examiner mischaracterized the teachings in Shou by suggesting that Shou teaches a digital filter where "the M multiple-stage shift registers do not have the same number of stages." As such, the Applicant submits that this provides additional reasons for the allowability of claim 44 over Shou.

In view of the foregoing, the Applicant submits that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)